

1       a an first comparator responsive to a first address  
2 signal group and to first control signals, the first  
3 comparator determining when one of a plurality selected  
4 characteristics are present in the first address signal  
5 group;

6       A second comparator responsive to a second address  
7 signal group and to second control signals, the second  
8 comparator determining when a second of the plurality of  
9 selected characteristics is present in the second address  
10 signal group; ~~and~~

11       ~~a second~~ an inter-comparator conductor, the ~~second~~  
12 inter-comparator conductor applying an indicia of an  
13 identification of the second selected characteristic to the  
14 first comparator, the first comparator generating an event  
15 signal when the first and the second selected  
16 characteristics are ~~identified~~ present; and

17       a data qualification unit coupled to the first  
18 and second comparators, the data qualification unit  
19 receiving architecture status signals from the processor,  
20 the data qualification unit applying enabling signals to  
21 the first and second comparators.

22  
23       2.     **(Previously Amended)**       The comparator unit as  
24 recited in claim 1 wherein the first and the second address  
25 signal groups are the same address signal group.

1 Please amend Claim 3 as follows.

2  
3 3. (Currently Amended) The comparator unit as recited  
4 in claim 1 wherein the first and second selected  
5 characteristics are selected from the group consisting of  
6 an exact characteristic, a touching characteristic, a  
7 touching less than the address signal characteristic and a  
8 touching greater than the address signal characteristic.

9  
10 Please cancel Claim 4.

11  
12 4. (Cancelled) ~~The comparator unit as recited in~~  
13 ~~claim 1 further comprising a data qualification unit, the~~  
14 ~~data qualification unit providing an enabling signal when~~  
15 ~~the data accessed by the associated address has a~~  
16 ~~predetermined relationship.~~

17  
18 5. (Original) The comparator unit as recited in  
19 claim 1 wherein either one of the first and the second  
20 comparator can generate an event signal when at least one  
21 of a touching requirement and an exact requirement is  
22 satisfied by an applied address signal group.

23  
24 Please amend Claim 6 as follows.

25  
26 6. (Currently Amended) A comparator unit for use in  
27 a test and debug system for a processing unit; the  
28 comparator unit comprising:

29 a first comparator and a second comparator, each  
30 comparator including:

1 a comparison logic unit for comparing an input  
2 address signal group with a control address signal group to  
3 determine when a selected one of a plurality of  
4 characteristics is present; and  
5 an intercomparator conductor for providing the  
6 results in one comparator to the other comparator;  
7 a data qualification unit coupled to the first  
8 and second comparators, the data qualification unit  
9 receiving architecture status signals from the processing  
10 unit, the data qualification unit applying enabling signals  
11 to the first and second comparator; and  
12 an event signal generation unit, the comparison  
13 logic unit applying a signal to the event generation  
14 unit ~~and to the event signal generation unit of the other~~  
15 comparator when the selected characteristic is identified,  
16 the event generation unit generating an event signal when  
17 the signals from the two comparators have ~~predetermined~~  
18 ~~values identifying~~ identified the selected characteristic  
19 associated in each comparator both comparators.

20  
21 **Please cancel Claim 7.**

22  
23 7. **(Cancelled)** ~~The comparator unit as recited in~~  
24 ~~claim 6 wherein each comparator includes a data qualifying~~  
25 ~~unit, the data qualifying unit responsive to an input~~  
26 ~~signal, the input signal determining when a pre-established~~  
27 ~~signal group has certain characteristics, the data~~  
28 ~~qualifying unit applying a control signal to the comparison~~  
29 ~~logic unit determining whether generation of an event~~  
30 ~~signal is enabled.~~

1     **Please amend Claim 8 as follows.**

2  
3           8.     **(Currently Amended)** The comparator unit as recited  
4 in claim 6 wherein the, ~~the~~ selected characteristics are  
5 selected from a group consisting of an exact characteristic  
6 and a touching characteristic.

7  
8           9.     **(Original)**     The comparator unit as recited in  
9 claim 8 wherein the address signal groups are the same  
10 signal group.

11  
12          10.    **(Previously Amended)** The comparator unit as  
13 recited in claim 6 wherein the selected characteristics are  
14 entered in the comparison logic unit by control signals.

15  
16          11.    **(Original)**     The comparator as recited in claim  
17 10 wherein each comparator can operate independently, each  
18 comparator capable of generating an event signal in  
19 response to at least one of a touching requirement and an  
20 exact requirement.

21  
22     **Please amend Claim 12 as follows.**

23  
24          12.    **(Currently Amended)** In a host processing unit, the  
25 method of determining when a first and a second input  
26 address signal group each meets at least one selected  
27 characteristic, the method comprising:  
28         qualifying the first input address signal group;

1       determining in a first comparator when the first  
2   input signal group has a first selected characteristic  
3   relative to a first reference address;  
4       qualifying the second input address signal group;  
5       determining in a second comparator when the second  
6   input address signal group has a second selected  
7   characteristic relative to a second reference address;  
8       coupling the results of the first comparator and the  
9   second comparator; and  
10      generating an output signal when the first and the  
11   second predetermined conditions are met, the output signal  
12   controlling the operation of ~~the~~ a host processor.

13  
14   **Please amend Claim 13 as follows.**

15  
16       13.   **(Currently Amended)** The method as recited in  
17   claim 12 further comprising identifying the position in the  
18   program execution with a program counter signal, the  
19   program counter signal being one of the address signal  
20   groups.

21  
22   **Please cancel Claim 14.**

23  
24       14.   **(Currently Cancelled)** ~~The method as recited in~~  
25   ~~claim 12 further comprising applying a signal from a data~~  
26   ~~qualification unit indicating that the data signal group~~  
27   ~~accessed at the input address signal group has a~~  
28   ~~predetermined relationship.~~

1 Please cancel Claim 15.

2  
3 15. (Currently Cancelled) ~~The method as recited in~~  
4 ~~claim 14 wherein the predetermined relationship is~~  
5 ~~determined by the relationship to a reference data value.~~

6  
7 16. (Previously Amended) The method as recited in  
8 claim 12 further comprising applying a signal to the  
9 comparators indicative of an associated signal group  
10 characteristic, the signal controlling generation of the  
11 output signal.

12  
13 Please amend Claim 17 as follows.

14  
15 17. (Currently Amended) In a target processor,  
16 apparatus for generating a trigger signal, the apparatus  
17 comprising:

18 a plurality of event signal generating units, wherein  
19 at least one of the event signal generating units is a  
20 comparator unit, the comparator unit including:

21 a first comparator and a second comparator, each  
22 comparator having:

23 a comparison logic unit for comparing an  
24 input address signal group with a control signal group to  
25 determine when one of a plurality of selected  
26 characteristics is present;

27 an inter-comparator conductor for  
28 communicating the results of one comparator to the other  
29 comparator; and

1 an event signal generating unit, the  
2 comparison logic unit applying a signal to the  
3 event generating unit and to the event signal generating  
4 unit of the second comparator when the selected  
5 characteristic is identified, the event generating unit  
6 generating an event signal when the signals from the two  
7 comparator logics have predetermined logic values;

8 a data qualification unit coupled to the first and  
9 second comparators, the data qualification unit receiving  
10 architecture status signals from the target processor, the  
11 data qualification unit applying enabling signals to the  
12 first and second comparators; and

13 a trigger generation unit coupled to the plurality of  
14 event signal generation units, the trigger generation unit  
15 responsive to at least one preselected event signal for  
16 generating a ~~an associated~~ trigger control signal, the  
17 trigger generation unit generating a trigger control signal  
18 for initiating a test procedure.

19  
20 18. **(Previously Amended)** The target processor as  
21 recited in claim 17 wherein the comparator unit receives a  
22 program counter address input signal identifying the  
23 position in the program execution.

24  
25 **Please amend Claim 19 as follows.**

26  
27 19. **(Currently Amended)** The target processor as  
28 recited in claim 17 wherein one comparator receives a  
29 program counter address counter address input signal and

1 the second comparator receives an address signal group  
2 referenced by the program counter address.

3  
4 20. **(Currently Amended)** The target processor as  
5 recited in claim 17 wherein the preselected condition is  
6 selected from the group consisting of a touching  
7 requirement, an exact requirement, a touching requirement,  
8 a touching less than the address signal requirement and a  
9 touching greater than the address signal requirement.